Implanted Bottom Gate for Epitaxial Graphene on Silicon Carbide

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Abstract. We present a technique to tune the charge density of epitaxial graphene via an electrostatic gate that is buried in the silicon carbide substrate. The result is a device in which graphene remains accessible for further manipulation or investigation. Via nitrogen or phosphor implantation into a silicon carbide wafer and subsequent graphene growth, devices can routinely be fabricated using standard semiconductor technology. We have optimized samples for room temperature as well as for cryogenic temperature operation. Depending on implantation dose and temperature we operate in two gating regimes. In the first, the gating mechanism is similar to a MOSFET, the second is based on a tuned space charge region of the silicon carbide semiconductor. We present a detailed model that describes the two gating regimes and the transition in between.

1. Introduction

The fascination of graphene lies in many scientific and technological specialties, including a linear dispersion relation, a nontrivial structure of the electronic wave function and unprecedented charge carrier mobilities [1, 2, 3]. Furthermore it is a well-defined two dimensional electron gas residing openly at the surface. Hence it can be manipulated chemically and physically with, in principle, atomic resolution. Graphene provides an opportunity to investigate electronic transport and surface science spectroscopy on the same material [4, 5, 6, 7, 8]. Varying the charge density in graphene permits the exploration of many phenomena [1, 6, 9]. For the commonly used exfoliated graphene, this can easily be achieved by employing the silicon substrate as an electrostatic bottom gate and its oxide as the dielectrics. However, exfoliated graphene flakes have limitations in size and reproducibility.

Epitaxial graphene has turned out to share the interesting properties of exfoliated graphene and is routinely fabricated in excellent qualities on large areas [10, 11]. Since SiC is a wide-bandgap semiconductor material, the use of the substrate as bottom gate is manifest, however technically not easy to achieve. Both highly insulating material and well conducting gate electrode have to be monolithically implemented, and this setup has further to serve as source for graphene growth. As a work-around, in some surface science experiments the charge carrier density in epitaxial graphene is controlled by applying specific ad-atoms as a static top gate [12, 13].

We present a setup for bottom gated epitaxial graphene by means of ion implantation into a semiinsulating SiC wafer with subsequent graphene growth. In this way, a conductive layer is created which is separated from the graphene by an insulating region. In [14] we showed that with this setup the charge carrier density in so called 'quasi-freestanding monolayer graphene' (QFMLG) obtained via hydrogen intercalation [15, 16] can be efficiently tuned. By adjusting the implantation energy E_I and the implantation dose D_I, the capacitance of the bottom gate as well as the optimum working temperature can be tailored. In this article we want to complement the previous publication [14] by (i) investigating the practical limits of implantation doses and a comparison of the implantation species nitrogen and phosphor and (ii) explaining the operation principle in detail by a specifically adapted model, which is (iii) supported by experiments under UV illumination. A striking feature in reference [14] was the observation of two different operation regimes. In the so called implanted plate capacitor (IPC) regime, that is observed for low temperatures, the situation is equivalent to a simple plate capacitor and the capacitance does not depend on gate voltage V_g. In the Schottky capacitor (SC) regime, that is observed for elevated temperatures, the physics is governed by the graphene/SiC Schottky contact. The SC regime shows improved gate coupling and a dependence of the capacitance on V_g. The model in section 3.2 describes the two gating regimes as well as the transition in between. UV illumination provides a control parameter to force the system into the SC regime, even at low temperature (see section 3.3).

Table 1. Implantation species, dose D_I and energy E_I, the distance from the gate to the surface d, the theoretical and measured capacitance in the IPC regime and the typical breakdown voltage at room temperature V_{bd} for the presented samples.

	element	D_I (cm^{-2})	E_I (MeV)	d (µm)	C_{IPC} (nF cm^{-2})	$C_{IPC,m}$ (nF cm^{-2})	V_{bd} (V)
S1	N	$8.0 \cdot 10^{12}$	1.0	0.8	11	11.4	> 160
S2	N	$3.3 \cdot 10^{13}$	1.0	0.7	12	12.5	≈ 100
S3	N	$3.0 \cdot 10^{14}$	2.0	1.0	8.5	6.8	≈ 20
S4	N	$3.0 \cdot 10^{14}$	2.0	1.0	8.5	8.6	≈ 20
S5	P	$8.0 \cdot 10^{14}$	2.0	0.6	14	8.5	≈ 15

2. Sample preparation and experimental details

Our devices were fabricated on commercial on-axis, semi-insulating 6H-SiC (0001) wafers with a vanadium (V) compensation of $[V] \approx 10^{17}\,\text{cm}^{-3}$. The samples were hydrogen etched at $T = 1520\,°C$ to remove surface polishing damage similar to the process described in [11]. The conductive layer used as the bottom gate was created by means of ion implantation of nitrogen (N) or phosphor (P), which are shallow donors in SiC. The implantation profile that can be calculated using the Monte-Carlo simulation TRIM (Transport of Ions in Matter) [17] has its maximum at $z_{max} = 1.0$–$1.4\,µm$ depending on the implantation energy E_I and drops exponentially towards the surface. The SiC becomes conductive at a depth d and below, where the doping concentration overcompensates the V concentration. This leads to the simultaneous formation of a conductive gate electrode with a maximum donor concentration $[D]_{gate}$ and an 'insulating layer' with thickness d between the gate electrode and the surface (figure 1). Here, we report on five samples (S1 to S5) with different implantation doses, energies and species (see table 1). The bottom gate is connected to the surface with two vertical channels as described in [14]. For the activation of the implanted dopants the samples were heated for 15–30 min at temperatures between $T = 1550\,°C$ and $T = 1700\,°C$ followed by a 90 s hydrogen etch at $T = 1520\,°C$ to remove surface damage caused by the implantation. For the growth of epitaxial graphene on SiC (0001) the process described in [15] is used to obtain hole doped QFMLG that is decoupled from the substrate by hydrogen intercalation. As shown in [14] only due to the intercalation step that saturates dangling bonds at the SiC/graphene interface [15], the charge carrier density in the graphene can be tuned using the bottom gate. Using standard e-beam lithography and reactive ion etching graphene was patterned in Hall bar structures similar to the process described in [8].

Micro-Raman spectra were measured under ambient conditions using a triple spectrometer with a liquid N_2 cooled CCD-detector. For excitation a frequency doubled Nd:YVO$_4$ laser with a wavelength of 532 nm was focused on the sample by a 100× objective.

Transfer characteristics and Hall measurements were either performed in a

continuous-flow cryostat using magnetic fields of ± 0.66 T at temperatures between 29 K and 300 K or in a Oxford cryostat with a minimal temperature of 1.4 K and a magnetic field of up to 8 T. The AC differential capacitance $C_{\text{diff,AC}}$ measurements were performed using a LCR meter at a frequency $f = 1$ kHz (PSM1735 NumetriQ). The DC capacitance C_{DC} was obtained by measuring the Hall resistance R_{H} at gate voltages $V_{\text{g}} = 0$ V and $V_{\text{g}} = 3$ V with

$$C_{\text{DC}} = \frac{1}{3\,\text{V}} \left(\frac{1}{R_{\text{H}}(V_{\text{g}} = 0\,V)} - \frac{1}{R_{\text{H}}(V_{\text{g}} = 3\,V)} \right) \tag{1}$$

For the UV illumination a commercial UV-Diode with a wavelength of $\lambda = 390$ nm and an optical power of $P = 2.2$ mW was mounted roughly 1 cm above the sample.

3. Experimental results and discussion

Raman measurements were performed to investigate the influence of implantation induced damage on the quality of the subsequently grown graphene. Figure 2 compares the Raman signal of sample S4 with the signal of QFMLG grown on our standard SiC substrate without implantation. The spectra show three prominent peaks at about 1340 cm^{-1}, 1584 cm^{-1} and 2670 cm^{-1} called D-, G- and 2D-band, respectively. In both spectra, the narrow 2D-line is very well described by a single Lorentzian which is typical of monolayer graphene [18]. Furthermore, the intensity ratio $I(D)/I(G)$, which is related to defects in graphene [19], is similar. Thus, no negative influence of the implantation on the graphene quality is observed. This is complemented by the fact that the electrical properties of samples with and without implanted gate are comparable (typical hole densities are in the range of $(2\text{–}6)\cdot 10^{12}$ cm^{-2} and the typical mobility is $\mu \approx 3000$ cm^2/Vs).

3.1. Exploring the limits of implantation doses

First we address the question, which minimal implantation dose is needed to fabricate a working bottom gate. As the gate layer is implanted through the insulating layer, using a D_{I} as low as possible is favorable as it minimizes implantation induced damage and therefore leakage current. Obviously for a conducting gate electrode $[D]_{\text{gate}}$ has to exceed the vanadium concentration. In addition, $[D]_{\text{gate}}$ has to be high enough that the gate is not depleted at high gate voltages. The depletion occurs at a V_{g}, for which the induced charge carrier density n_{ind} becomes as large as the uncompensated donor areal density D_{net} in the gate layer:

$$n_{\text{ind}} = C_{\text{IPC}} V_{\text{g}}/e \doteq D_{\text{net}}. \tag{2}$$

$C_{\text{IPC}} = \varepsilon_{\text{SiC}} \varepsilon_0 / d$ is the capacitance of the bottom gate in the IPC regime with d determined by TRIM simulation. For the dielectric constant of 6H-silicon carbide we used $\varepsilon_{\text{SiC}} = 9.7$ [20]. D_{net} is given by

$$D_{\text{net}} = \int_{z}^{z'} c \cdot [D] - [V] \mathrm{d}\zeta, \tag{3}$$

where z or z' denotes the depth at which [D] exceeds or drops below [V], respectively. c denotes the percentage of the implanted donors which are electrically activated during the annealing step.

To illustrate the consequences of a depleted gate layer we compare the gate response of the differential capacitance $C_{\text{diff,AC}}$, the conductivity σ and the leakage current I_{g} of samples S1 and S2. For S1, D_{I} was chosen such that $[D]_{\text{gate}} \approx 6 \cdot 10^{17}\,\text{cm}^{-3} \approx 6 \cdot [V]$ (figure 1a). A roughly four times larger D_{I} was used for sample S2 (table 1). The implantation dose D_{I} is low enough that both samples operate in the IPC regime up to room temperature. The gate layer of S1 becomes depleted at $V_{\text{g}} \approx 45\,\text{V}$, which leads to a steep drop of $C_{\text{diff,AC}}$ (figure 3a). In addition, the dependence of σ on V_{g} changes from linear to sub-linear and becomes nearly independent from V_{g} for $V_{\text{g}} > 60\,\text{V}$. Also at $V_{\text{g}} \approx 45\,\text{V}$ a kink in I_{g} is observed (figure 3b,c). This results from the drastically increased resistivity of the gate layer caused by the depletion. In this regime, if V_{g} is increased, the additional voltage ΔV_{g} drops mainly laterally in the highly resistive gate layer. As a consequence, first the induced charge per volt in the graphene layer and thus $C_{\text{diff,AC}}$ is decreased explaining the behaviour of σ. Second, the series resistance for the leakage current is increased, which shows up in the decreased slope of $I_{\text{g}}(V_{\text{g}})$. The gate voltage $V_{\text{g}} = 45\,\text{V}$ at which the gate layer becomes depleted can be calculated in agreement with the experiment using equations 2 and 3 with $c = 0.7$, which is close to values from literature [21].

In contrast, for sample S2 $C_{\text{diff,AC}}$ is independent of V_{g} and thus no depletion of the gate layer is observed throughout the investigated gate voltage range. Therefore, $\sigma(V_{\text{g}})$ shows the linear behaviour typical for graphene [1]:

$$\sigma(V_{\text{g}}) = e\mu n(V_{\text{g}}) = e\mu(n_0 - \frac{C_{\text{IPC}}}{e}V_{\text{g}}). \tag{4}$$

Here it is assumed that the mobility μ is independent from charge carrier density n, and n_0 is $n(V_{\text{g}} = 0)$. Note that the above formula is only valid if the Fermi level is sufficiently far away from the Dirac point so that only one type of charge carriers contributes to the current. Also I_{g} shows the expected behavior typical for an insulator with a breakdown voltage $V_{\text{bd}} \approx 100\,\text{V}$. Note that all measurements shown were carried out with $V_{\text{g}} < V_{\text{bd}}$. Therefore I_{g} does not affect the measurements, as it is always orders of magnitude smaller than the source-drain current I_{SD}, which is typically in the μA range. For S2 equations 2 and 3 yield depletion of the gate layer at $V_{\text{g}} = 260\,\text{V}$, which is much larger than the breakdown voltage and is thus not reached.

The fact that for $V_{\text{g}} < 100\,\text{V}$ S1 shows higher leakage currents than S2 is not attributed to the difference in implantation dose but to the local wafer quality. Probably the wafer area, of which S1 was fabricated, had a higher defect density than S2. Indeed, for $V_{\text{g}} < V_{\text{bd}}$ we observe similar sample to sample fluctuations of I_{g} between samples fabricated on the same chip. In contrast, the breakdown voltage V_{bd} depends on both implantation dose D_{I} and wafer quality. Larger D_{I} leads to smaller V_{bd} (e.g. for S4: $V_{\text{bd}} \approx 20\,\text{V}$). Hence, an optimal gate performance in the IPC regime is achieved when the gate voltage at which the gate layer becomes depleted and the breakdown voltage

are similar. This can be controlled via D_I.

It is remarkable that for all N-implanted samples the measured capacitance in the IPC regime $C_\mathrm{IPC,m}$ is in good agreement with the calculated C_IPC using a simple plate capacitor model. This shows that for samples S1 to S4 defects in the insulating layer or traps at the graphene/SiC interface have no influence on the capacitance in the IPC regime. Only for S5 using P for the gate layer the expected and the measured capacitance differ significantly (table 1). We assign this to a partial shielding of the gate effect by implantation induced defects in the insulating layer. This effect is suspected to be more important for P- than for N-implantation as the P^+ ions are much heavier and thus create more damage.

Now, we address the low-temperature limit of the bottom gate operation. Below a characteristic threshold temperature T_th the above used gate freezes out and becomes insulating ($T_{th} \approx 75\,\mathrm{K}$ for sample S2)[14]. Therefore, a higher doping concentration in the gate layer is needed to maintain a finite conductivity at low T, ideally a quasi-metallic conductivity governed by an impurity band is used. However, the N doping in SiC is limited to $[N] \approx 3 \cdot 10^{19}\,\mathrm{cm}^{-3}$ [22], which leads to a minimal operation temperature of $T_\mathrm{th} \approx 6\,\mathrm{K}$ (figure 4 inset). As the maximal solubility of P in SiC is roughly one order of magnitude higher as for N [22] the change of the donor species allows for a higher maximal dopant concentration (for S5: $[P]_{max} = 4 \cdot 10^{19}\,\mathrm{cm}^{-3}$) and therefore a lower T_th. We observe that the gate of S5 works at least down to $T = 1.4\,\mathrm{K}$. With this set of implantation parameters used for S5 a bottom gated device can be continuously used from low temperatures up to room temperature. From our perspective a further increase of D_I is not advantageous as high doping of the gate layer brings along several limitations. First, a high D_I decreases the breakdown voltage V_bd. At elevated temperatures this is fortunately counterbalanced by the appearance of the SC regime (see below). Second, a partial shielding of the gate effect by implantation induced defects in the insulating layer is observed. For N-implanted samples this manifests as a saturation of the gate effect at higher V_g. For P-implanted samples a partial shielding independent of V_g is observed. Nevertheless, P-implanted samples allow for a much wider range of accessible charge carrier densities in graphene at low T than N-implanted samples (figure 4). The capacitance $C_\mathrm{IPC,m}$ of sample S5 determined from the fit in figure 4 is still $C_\mathrm{IPC,m} = 5.3\,\mathrm{nF/cm}^{-2}$ at $T = 4.2\,\mathrm{K}$, compared to $C_\mathrm{IPC,m} = 9.1\,\mathrm{nF/cm}^{-2}$ at $T = 225\,\mathrm{K}$, where the gate electrode is well conducting but the sample still in the IPC regime.

3.2. Modeling the different gating regimes

When increasing the temperature to $300\,\mathrm{K}$ for sample S3 to S5 a transition from the IPC to the SC regime is observed. It manifests itself in a strong and steep increase of C_DC at the transition temperature T_t (figure 5). We used a DC measurement to determine the capacitance C_DC in the SC regime, as the time constant of the gate response is of the order of seconds (figure 5 inset) and thus an AC measurement would underestimate

the capacitance. For S4 we find $T_t \approx 270\,\text{K}$ for S5 $T_t \approx 250\,\text{K}$.

The two regimes as well as the transition can be understood by calculating the temperature dependent voltage drop of V_g along the insulating region between the gate electrode and the surface. In contrast to standard MOSFETs where the voltage drops homogeneously along the dielectric layer, the voltage drop in our devices is non-trivial. Due to the Schottky contact at the graphene/SiC interface V_g divides into two parts:

$$V_g = V_{SC} + V_{IPC}. \tag{5}$$

V_{SC} drops at the Schottky contact and V_{IPC} is the standard voltage drop across a plate capacitor (figure 1). In the SC regime($T \gg T_t$) when the resistivity of the SiC is low the whole gate voltage drops along the space charge region (SCR) of the Schottky contact ($V_g = V_{SC}$). In the IPC regime ($T \ll T_t$), however, the resistivity of the insulating layer is high and the voltage drop is equivalent to a plate capacitor ($V_g = V_{IPC}$). Here, the Schottky contact can be neglected. The transition from the IPC to the SC regime is caused by the different temperature dependences of $V_{SC}(T)$ and $V_{IPC}(T)$. To model these temperature dependences we calculate the current density across a Schottky contact I_{SC} under reverse bias, given by

$$I_{SC}(T) = A^*_{fit} T^2 \exp\left(\frac{-\Phi_{b,eff}}{k_B T}\right) \left(\exp\left(\frac{qV_{SC}}{k_B T}\right) - 1\right), \tag{6}$$

with $\Phi_{b,eff}$ being the effective Schottky barrier height. A^*_{fit} is the fitted effective Richardson constant of the Schottky contact. We can determine $\Phi_{b,eff}$ and A^*_{fit} by fitting equation 6 to the measured $I_g(T)$ in the SC regime. The resistive voltage drop V_{IPC} along the insulating layer is then obtained by

$$V_{IPC}(T) = d\rho_{SiC}(T) I_{SC}(T). \tag{7}$$

The resistivity of the insulating layer $\rho_{SiC}(T)$ is determined with $\rho_{SiC}(T) = \rho_0 \exp(E_V/(k_B T))$ with $E_V = 0.7\,\text{eV}$ being the activation energy of the vanadium acceptor level. ρ_0 is obtained from measuring I_g in forward direction of the Schottky contact at room temperature, where I_g is only determined by the resistivity of the insulating layer. Combining equations 5 to 7 $V_{SC}(T)$ can be calculated by solving

$$V_g = V_{SC} + d\rho_0 \exp\left(\frac{E_V}{k_B T}\right) I_{SC}(T) \tag{8}$$

numerically for a given V_g and T.

The overall capacitance C_{DC} has two contributions. The first arises from the charge accumulated in the gate electrode, the second from the additional charge in the SCR of the Schottky contact

$$C_{DC} = \frac{e}{V_g} \left(\frac{\varepsilon_{SiC}\varepsilon_0}{ed} V_{IPC} + (w - w_{min})N_d\right), \tag{9}$$

with the thickness of the SCR $w = \sqrt{2\varepsilon_{SiC}\varepsilon_0(V_{SC} + V_{bi})/(eN_d)}$ and $w_{min} = w(V_{SC} = 0)$. V_{bi} is the built-in voltage of the graphene/SiC Schottky contact that was measured using X-ray photo electron spectroscopy (XPS) as described in reference [23]. N_d is the charge density in the SCR. All parameters of the model except N_d were determined

Table 2. Parameters of the model. The experimentally obtained values and the values used for the fit in figure 5 are shown.

	V_{bi} (eV)	$\Phi_{\text{b,eff}}$ (eV)	A^*_{fit} (nA K^{-2})	ρ_0 (Ωm)	N_{d} (10^{16} cm^{-3})
S4 meas.	0.9 ± 0.1	0.13 ± 0.03	$(1.0 \pm 1.3) \cdot 10^{-3}$	$(2.2 \pm 1.9) \cdot 10^{-4}$	-
S4 fit	0.9	0.14	$1.1 \cdot 10^{-3}$	$9.5 \cdot 10^{-5}$	3.1
S5 meas.	0.9 ± 0.1	0.56 ± 0.03	$(1.2 \pm 1.4) \cdot 10^{4}$	$(1.2 \pm 0.8) \cdot 10^{-4}$	-
S5 fit	0.9	0.53	$4.3 \cdot 10^{3}$	$3.5 \cdot 10^{-4}$	4.5

from separate experiments (see table 2). N_{d} was obtained by fitting the model to the measured $C_{\text{DC}}(T)$ (figure 5). ‡ Extracting I_0 and $\Phi_{\text{b,eff}}$ simultaneously from a fit to I_{g} using equation 6 is problematic as I_0 is very sensitive to a change of $\Phi_{\text{b,eff}}$. This leads to a large error in I_0 (table 2). To obtain I_0 for the model, we first chose a $\Phi_{\text{b,eff}}$ and then determined I_0 using equation 6 with fixed $\Phi_{\text{b,eff}}$. To optimize the match of the model to the data of sample S4 we varied some of the parameters within the experimental error. For the phosphorus doped sample S5 we included partial shielding of the gate effect by implantation related defects (otherwise the capacitance in the IPC regime would be too large. See table 1). The measured ρ_0 turned out to yield a too small transition temperature T_{t} for sample S5. We therefore used a somewhat higher value. The parameters used for the fits in figure 5 are shown in table 2. Note that T_{t} is independent of the choice of N_{d} and hence depends only on separately measured quantities.

In the SC regime the differential capacitance of the gate depends on V_{g}. With increasing V_{g} the SCR becomes larger and thus the differential capacitance decreases. Hence, the induced charge carrier density n_{ind} becomes sub-linear. Figure 6a shows that for small V_{g} we find excellent agreement with the calculated n_{ind} at room temperature using the textbook formula

$$n_{\text{ind}}(V_{\text{g}}) = \sqrt{2\varepsilon_{\text{SiC}}\varepsilon_0 N_{\text{d}}/e} \left(\sqrt{V_{\text{g}} + V_{\text{bi}}} - \sqrt{V_{\text{bi}}} \right). \tag{10}$$

For $V_{\text{g}} > 9$ V the measured n_{ind} is slightly smaller as the theoretically predicted values. Probably this is caused by the filling of traps at high electric field that was already observed in [14].

3.3. Controlling the transition to the SC regime with light

To extend the SC regime to low temperatures we apply ultra violet (UV) light with a photon energy larger than the SiC band gap ($E_{\text{g}} = 3.0$ eV). The UV illumination creates

‡ Estimating the course of the quasi-Fermi level $E_{F,n}$ for electrons in the SCR following the way presented in [24] we find that in agreement with the fitted N_{d} the V donor level, that lies 1.5 eV below the conduction band, is not crossing $E_{F,n}$. A crossing would lead to an increased N_{d} with $N_{\text{d}} > [V]$ as the V would also contribute to the charge in the SCR.

additional free charge carriers in the insulating layer and its resistivity is decreased similar to the already discussed case of elevated temperatures. Figure 6b shows that with UV illumination $n_{\mathrm{ind}}(V_{\mathrm{g}})$ has the sub-linear behaviour typical for the SC regime also at $T = 35\,\mathrm{K}$. Again for small V_{g} the measured $n_{\mathrm{ind}}(V_{\mathrm{g}})$ is very well described by equation 10. From the fits shown in figure 6a and 6b we obtain $N_{\mathrm{d}} = 2.3 \cdot 10^{16}\,\mathrm{cm}^{-3}$ and $N_{\mathrm{d}} = 2.9 \cdot 10^{16}\,\mathrm{cm}^{-3}$, respectively. This is slightly smaller than N_{d} obtained from the fit in figure 5. We assign this to a slow degradation of the gate coupling as applying high gate voltages probably creates additional defects that shield the gate effect.

The overall picture is fully confirmed by the following observation: when switching off the UV light at low temperatures the sample remains in the SC regime. This is a consequence of the extremely high resistivity of the insulating layer at low temperatures without UV illumination. Under these conditions the charge can not rearrange to the IPC distribution. Figure 7 shows the response of I_{SD} on a change of V_{g} from $V_{\mathrm{g}} = 0\,\mathrm{V}$ to $V_{\mathrm{g}} = 3\,\mathrm{V}$ for $T = 100\,\mathrm{K}$ and $T = 35\,\mathrm{K}$ with the sample being illuminated with UV light. For both temperatures the sample is in the SC regime due to the UV light and the observed gate response of I_{SD} is similar. Upon switching the UV light off, at $T = 100\,\mathrm{K}$ I_{SD} increases indicating a reduction of the gate coupling and a transition from the SC to the IPC regime. At $T = 35\,\mathrm{K}$, however, no change in I_{SD} is observed and the sample stays in the SC regime for at least several hours. It is a nice property of the system that low temperatures measurements in the favorable SC regime are possible without the disturbing influence of UV light.

4. Conclusion

We present a scheme to create a bottom gate in epitaxial graphene devices by ion implantation prior to graphene growth. The SiC takes over the functionality of both the conducting gate layer and the insulating dielectric. We have shown that substantial changes in charge carrier densities can be achieved. In this paper we give a detailed description of the influence of various doping profiles on the graphene/SiC heterojunction. In particular we elucidate the practical limits of implantation doses. Furthermore a nearly parameter-free model is developed which describes the underlying physics with high accuracy. We find two regimes for the gate capacitance with the Schottky regime being more efficient. Using UV light we can force the system to the SC regime even at cryogenic temperatures. The implanted bottom gate allows qualitatively new experiments using epitaxial graphene.

Acknowledgments

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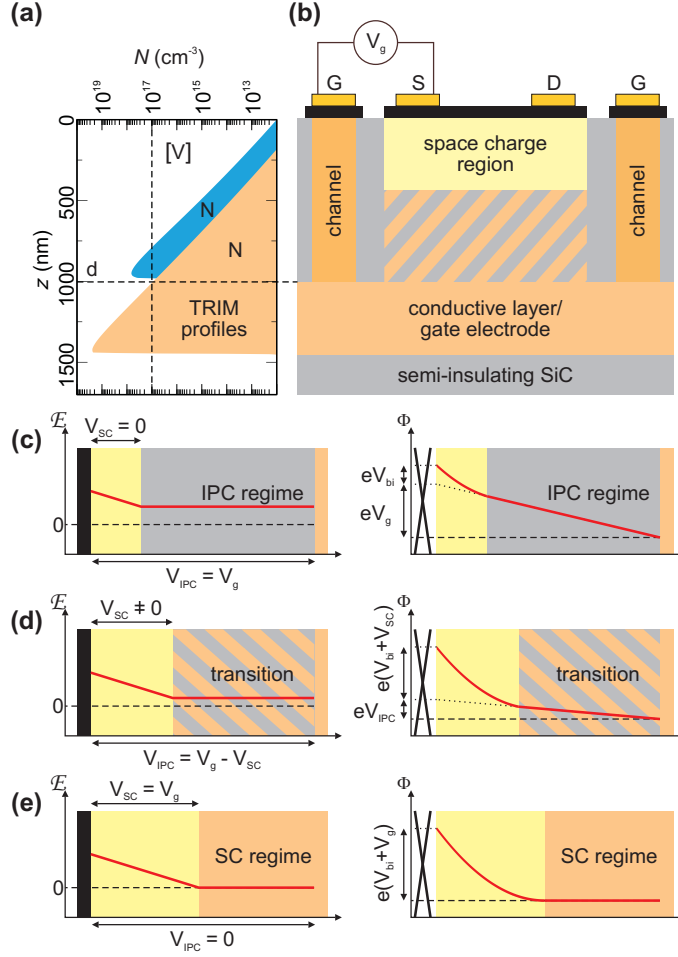
Figure 1. Scheme of the bottom gate. The conductive gate layer is created via implantation of nitrogen or phosphor ions in a depth d below the SiC surface. (a) TRIM simulation of the implantation profiles of S1 (blue) and S3 and S4 (orange). The SiC is conducting where the implanted dose exceeds the vanadium compensation $[V]$ (vertical, dotted line) and insulating elsewhere. The horizontal, dotted line indicates d for S3 and S4. (b) Setup of the bottom gate with source (S), drain (D) and gate (G) electrodes on graphene; conductive gate layer and implanted conductive channels. The area between the space charge region and the gate layer is insulating in the IPC regime whereas it is conducting in the SC regime. (c)–(e) Electric field and band diagram for this region in the different regimes. (c) In the IPC regime a constant electric field created by V_g is superimposed onto the built-in field of the depletion layer. (d) At the transition to the SC regime the constant electric field becomes smaller and the voltage drop along the space charge region increases. (e) In the SC regime the conductive layer extends up to the depletion layer. The whole gate voltage drops along the depletion layer.
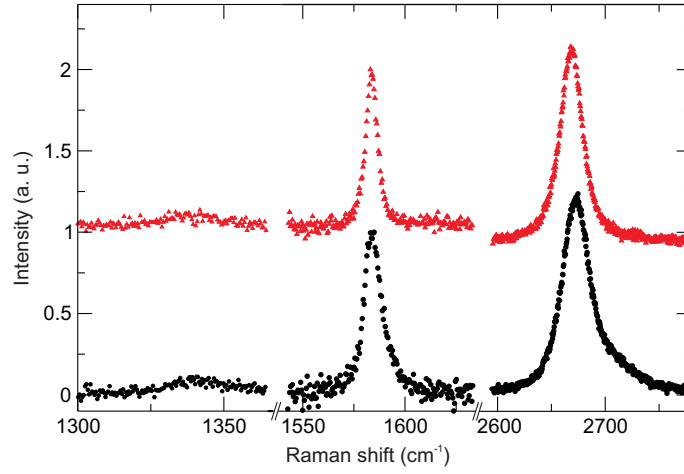
Figure 2. Raman spectra of QFMLG grown on pristine (circles) and implanted SiC (sample S4) (triangles). To remove the contribution of the substrate a SiC reference spectrum was subtracted. The spectra show the D-, G- and 2D band at $1340\,\mathrm{cm}^{-1}$, $1584\,\mathrm{cm}^{-1}$ and $2670\,\mathrm{cm}^{-1}$, respectively. The line widths of the G-peak are $6\,\mathrm{cm}^{-1}$ for S4 and $10\,\mathrm{cm}^{-1}$ for the pristine SiC, for the 2D-peak the line widths are $24\,\mathrm{cm}^{-1}$ and $31\,\mathrm{cm}^{-1}$, respectively. The spectrum of S4 is shifted along the intensity axis.
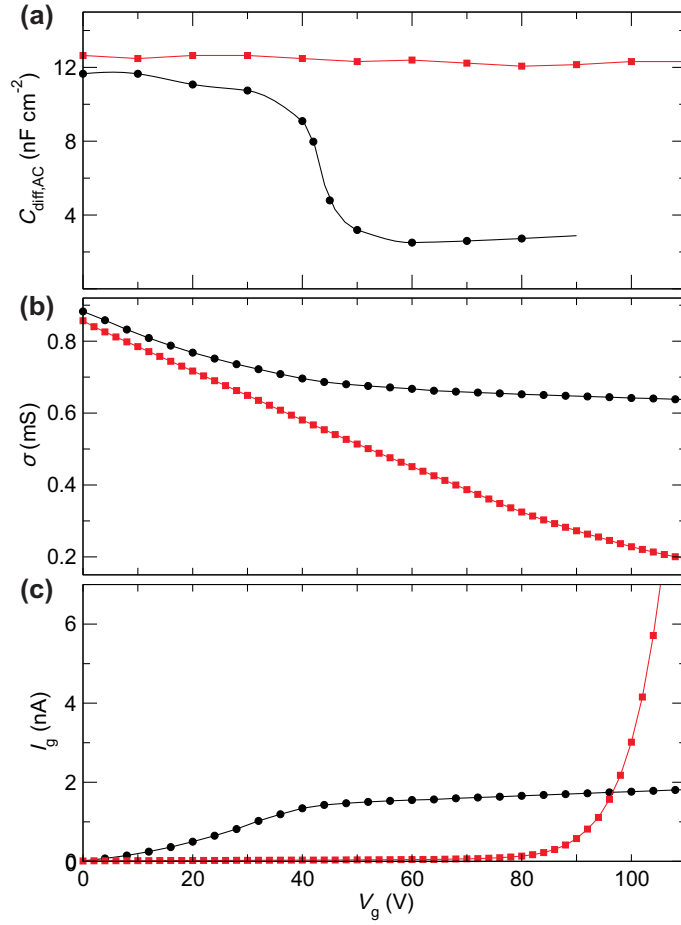
Figure 3. Gate response of S1 (circles) and S2 (squares). (a) The differential capacitance $C_{\mathrm{diff,AC}}$ of S1 shows a steep drop at $V_{\mathrm{g}} \approx 45\,\mathrm{V}$ due to the depletion of the gate layer. In contrast, $C_{\mathrm{diff,AC}}$ of S2 is independent of gate voltage. (b) For S1 a saturation of σ is observed for $V_{\mathrm{g}} > 60\,\mathrm{V}$, whereas σ of S2 shows a linear behaviour over the whole range of V_{g}. (c) Leakage current I_{g} of S1 shows a kink at $V_{\mathrm{g}} \approx 45\,\mathrm{V}$. I_{g} of S2 shows the typical behaviour of an insulator.
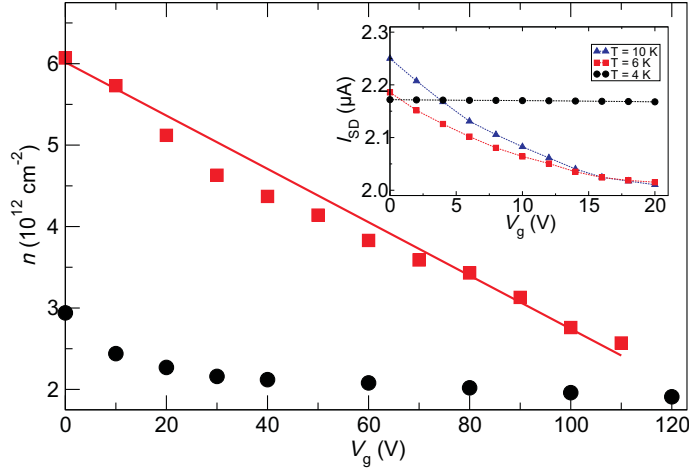
Figure 4. Change of carrier concentration n upon gate voltage V_g for S3 (circles) and S5 (squares) at low temperatures (for S3, $T = 6.0\,\mathrm{K}$ for S5 $T = 4.2\,\mathrm{K}$) and therefore in the IPC regime. For S3 only a small variation of n is achieved, whereas for S5 n could be changed by more than $3 \cdot 10^{12}\,\mathrm{cm}^{-2}$. The solid line shows a linear fit to the carrier concentration of S5. The inset shows the response of the source-drain current I_{SD} on gate voltage V_g of S3 for different temperatures. For $T \geq 6\,\mathrm{K}$ I_{SD} can be changed using the gate. For $T = 4\,\mathrm{K}$ the conductivity of the gate layer freezes out and no gate response of I_{SD} is observed.
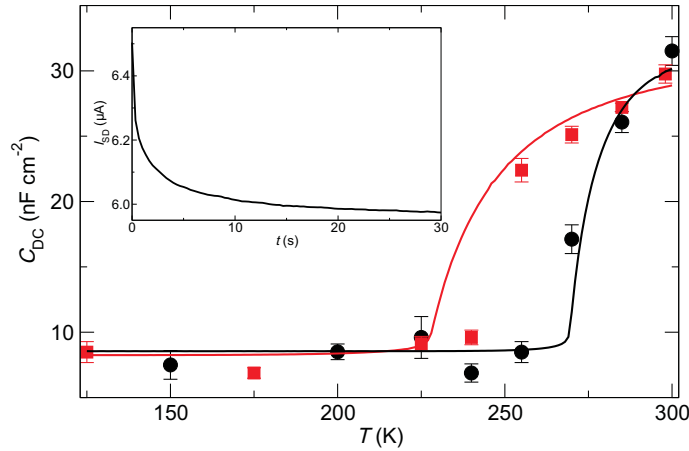

Figure 5. Temperature dependence of the capacitance C_{DC} of S4 (circles) and S5 (squares). Due to the transition from the IPC to the SC regime a strong increase of C_{DC} is observed. Solid lines show the calculated temperature dependence using the parameters from table 2. The inset shows the time-dependent response of the source-drain current I_{SD} of S5 on a change of the gate voltage from $V_g = 0\,\mathrm{V}$ to $V_g = 3\,\mathrm{V}$ at room temperature.
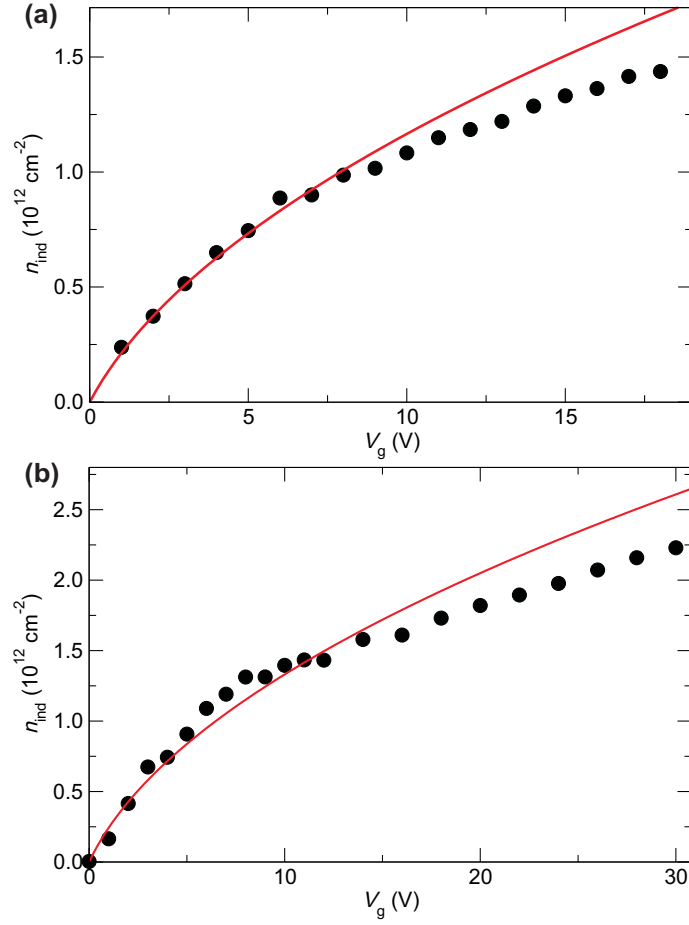
Figure 6. Measured (circles) and calculated (solid line) dependence of the induced charge carrier density $n_{\rm ind}$ on gate voltage for S4. (a) In the SC regime at room temperature. (b) With UV light illumination at $T = 35\,$K. The UV light allows to extend the SC regime to low temperatures.
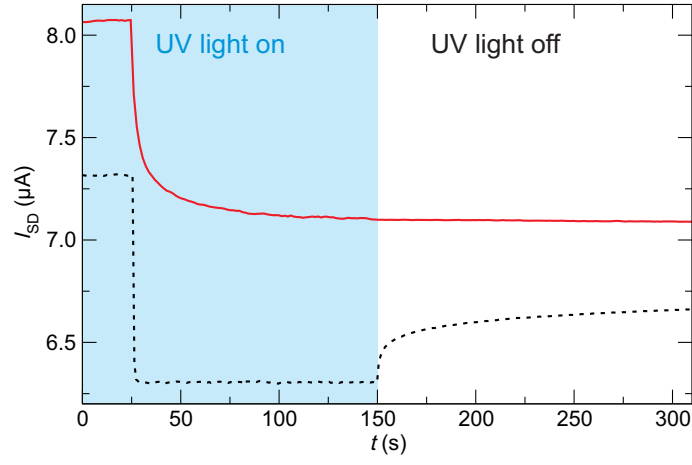
Figure 7. Gate response of the source-drain current I_{SD} of S4 at $T = 100\,\text{K}$ (dashed line) and $T = 35\,\text{K}$ (solid line). At the beginning of the measurement the sample is illuminated with UV light. At $t = 25\,\text{s}$ the gate voltage is changed from $V_g = 0\,\text{V}$ to $V_g = 3\,\text{V}$ and at $t = 150\,\text{s}$ the UV light is switched off. At $T = 100\,\text{K}$ the sample undergoes a transition back to the IPC regime whereas at $T = 35\,\text{K}$ it remains in the SC regime.